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# Ettus USRP B310 (OEM) Specifications

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# Ettus USRP B310 (OEM) Specifications

## Ettus USRP B310 (OEM) Specifications

These specifications apply to the Ettus USRP B310 (OEM) variant.

The Ettus USRP B310 has more than one form factor: USRP B310 (OEM), USRP B310 (Enclosed), and USRP B310 (PCIe). This document refers to the USRP B310 (OEM) variant. Refer to the specifications for your respective Ettus USRP B310 form factor for variant-specific information.

## Revision History

| Version    | Date changed | Description      |
|------------|--------------|------------------|
| 379307A-01 | August 2026  | Initial release. |

## Looking For Something Else?

For information not found in the specifications for your product, such as operating instructions, browse *Related Information*.

### Related information:

- [Ettus USRP B310 User Manual](#)
- [USRP B3xx Series Hardware Driver and Device Manual](#)
- [USRP B310 \(OEM\) Safety, Environmental, and Regulatory Information](#)
- [Software and Driver Downloads](#)
- [Dimensional Drawings](#)
- [Product Certifications](#)
- [Letter of Volatility](#)
- [Discussion Forums](#)
- [NI Learning Center](#)

## Definitions

*Warranted Specifications* describe the performance of a model under stated operating conditions and are covered by the model warranty.

*Characteristics* describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical**—describes the performance met by a majority of models.
- **Nominal**—describes an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured**—describes the measured performance of a representative model.

Values are *Measured* unless otherwise noted.

## Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Specifications are valid at 23 °C ambient temperature.<sup>1</sup>
- Specifications that reference dBFS are based on a full-scale digital level at the ADC or DAC interface.
- Specifications utilize default UHD 4.11.0 software configuration and a 122.88 MHz MCR (Master Clock Rate).

## Software

Table 1. Software

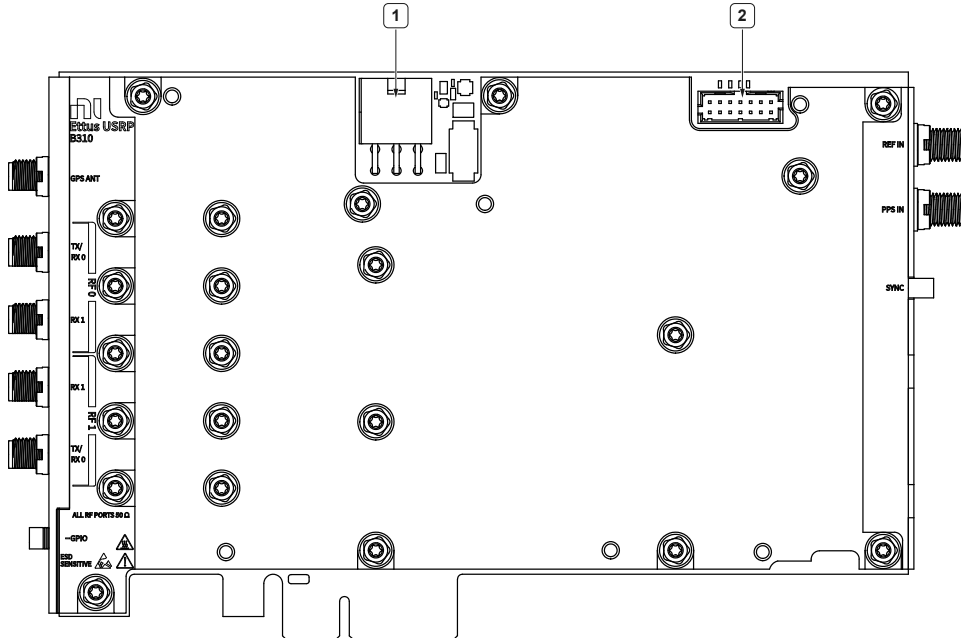
|                          |                                               |
|--------------------------|-----------------------------------------------|
| Device software          | USRP Hardware Driver™ version 4.11.0 or later |
| FPGA framework           | RFNoC                                         |
| Application environments | GNU Radio                                     |
| Programming languages    | C/C++, Python                                 |

1. The operating temperature is the recommended ambient temperature around the product with the PCIe variant integration (NI Part Number: 790817-01—PCIe). Higher operating temperatures might be achieved with active cooling such as fans or liquid cooling.

# USRP B310 (OEM) Front/Rear Panel

Overview of the front and rear panel elements of the Ettus USRP B310.

Figure 1. USRP B310 (OEM) Front/Rear Panels



1. AUX Power (J10)
2. JTAG (J13)

Table 2. Port/Connector Descriptions

| Port/Connector Name | Description                                                                              | Connector Type                                                                                                                                                            |
|---------------------|------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPS ANT             | Input for an external GPS antenna used by the onboard GPSDO.                             | <ul style="list-style-type: none"> <li>SMA (f), 50 <math>\Omega</math></li> <li>3.0 V, 0.19 W</li> </ul>                                                                  |
| TX/RX <0..1>        | Bidirectional radio frequency signal connector used for transmit and receive operations. | <ul style="list-style-type: none"> <li>SMA (f), 50 <math>\Omega</math></li> <li>RX—Receive only; +10 dBm input power damage level</li> <li>TX—+20 dBm, maximum</li> </ul> |

| Port/Connector Name | Description                                                                                      | Connector Type                                                                                                                                                                                                                              |
|---------------------|--------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RX <0..1>           | Radio frequency signal connector used for receive-only operations.                               | <ul style="list-style-type: none"> <li>SMA (f), 50 <math>\Omega</math></li> <li>RX—Receive only; +10 dBm input power damage level</li> </ul>                                                                                                |
| GPIO                | General purpose input/output digital terminals.                                                  | <ul style="list-style-type: none"> <li>Mini HDMI Type-C</li> <li>3.3 V output voltage</li> <li>250 mA VCC out, 8 mA per GPIO output port</li> <li>NOT AN HDMI-COMPATIBLE INTERFACE</li> </ul>                                               |
| Console JTAG (J13)  | For connecting to the FPGA for development and debugging. Provides access to JTAG.               | <ul style="list-style-type: none"> <li>2 V DC, maximum</li> </ul>                                                                                                                                                                           |
| SYNC                | For use with sharing a high-frequency reference and PPS across multiple Ettus USRP B310 devices. | <ul style="list-style-type: none"> <li>Mini HDMI Type-C</li> <li>Reference Clock Output—AC coupled output <math>\pm 0.325</math> V (0.65 V peak-peak)</li> <li>PPS Output—0 V to 3.3 V</li> <li>NOT AN HDMI-COMPATIBLE INTERFACE</li> </ul> |
| PPS IN              | Input for an external pulse-per-second (PPS) signal used for time synchronization.               | <ul style="list-style-type: none"> <li>SMA (f), 50 <math>\Omega</math></li> <li>+3.3 V, input only</li> </ul>                                                                                                                               |
| REF IN              | Input for an external 10 MHz reference clock signal used for frequency synchronization.          | <ul style="list-style-type: none"> <li>SMA (f), 50 <math>\Omega</math></li> <li><math>\pm 0.165</math> V to <math>\pm 0.45</math> V (0.33 V to 0.9 V peak-peak), input only</li> </ul>                                                      |

Figure 2. GPIO Connector Pinout

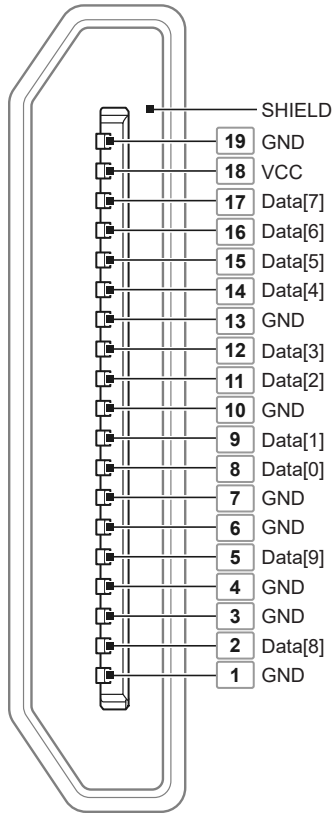


Table 3. GPIO Connector Pinout

| Pin | Name    | Direction | Voltage Domain | Description                                          |
|-----|---------|-----------|----------------|------------------------------------------------------|
| —   | SHIELD  | N/A       | N/A            | SHIELD                                               |
| 19  | GND     | N/A       | N/A            | Ground reference                                     |
| 18  | VCC     | Out       | +3.3 V         | External power for GPIO accessories (250 mA maximum) |
| 17  | Data[7] | In/Out    | 3.3 V          | General-purpose digital I/O                          |
| 16  | Data[6] | In/Out    | 3.3 V          | General-purpose digital I/O                          |
| 15  | Data[5] | In/Out    | 3.3 V          | General-purpose digital I/O                          |
| 14  | Data[4] | In/Out    | 3.3 V          | General-purpose digital I/O                          |

| Pin | Name    | Direction | Voltage Domain | Description                 |
|-----|---------|-----------|----------------|-----------------------------|
| 13  | GND     | N/A       | N/A            | Ground reference            |
| 12  | Data[3] | In/Out    | 3.3 V          | General-purpose digital I/O |
| 11  | Data[2] | In/Out    | 3.3 V          | General-purpose digital I/O |
| 10  | GND     | N/A       | N/A            | Ground reference            |
| 9   | Data[1] | In/Out    | 3.3 V          | General-purpose digital I/O |
| 8   | Data[0] | In/Out    | 3.3 V          | General-purpose digital I/O |
| 7   | GND     | N/A       | N/A            | Ground reference            |
| 6   | GND     | N/A       | N/A            | Ground reference            |
| 5   | Data[9] | In/Out    | 3.3 V          | General-purpose digital I/O |
| 4   | GND     | N/A       | N/A            | Ground reference            |
| 3   | GND     | N/A       | N/A            | Ground reference            |
| 2   | Data[8] | In/Out    | 3.3 V          | General-purpose digital I/O |
| 1   | GND     | N/A       | N/A            | Ground reference            |



**Note** The GPIO connector is not intended to drive large loads.

## Physical Characteristics

Table 4. Dimensions and Weight

| Parameter                      | Value                                                    |
|--------------------------------|----------------------------------------------------------|
| Dimensions, without connectors | 17.7 cm x 11.1 cm x 1.8 cm (7.0 in. x 4.4 in. x 0.7 in.) |
| Dimensions, with connectors    | 18.8 cm x 11.1 cm x 1.8 cm (7.4 in. x 4.4 in. x 0.7 in.) |
| Weight                         | 0.44 kg (0.97 lb)                                        |



**Note** For more information on product dimensions, visit [ni.com/dimensions](https://ni.com/dimensions), search by model number, and click the appropriate link.

## General Purpose I/O (GPIO)

Table 5. FPGA GPIO (through Mini HDMI Connector)

| Parameter              | Value                                     |
|------------------------|-------------------------------------------|
| GPIOs                  | 10                                        |
| GPIO I/O voltage       | +3.3 V                                    |
| GPIO input VIL/VIH     | 0.8 V, 2.0 V                              |
| Maximum rate           | 50 MHz (9 ns rise/fall time, typical)     |
| Maximum output current | 250 mA VCC Out, 8 mA per GPIO output port |

## Timing and Reference Connectors

Table 6. Mini HDMI Sync Port – Reference Clock and PPS Outputs

| Parameter                                            | Value                                              |
|------------------------------------------------------|----------------------------------------------------|
| Reference clock outputs                              | 4                                                  |
| PPS outputs                                          | 4                                                  |
| Recommended accessory                                | NI part number 791010-01 (Mini HDMI to 8 SMA's)    |
| Reference clock output voltage $V_{swing}$ , typical | AC-coupled output $\pm 0.325$ V (0.65 V peak-peak) |
| Reference clock output frequencies                   | 122.88 MHz or 125 MHz                              |
| PPS output voltage                                   | 0 V to +3.3 V                                      |

Table 7. RefClk IN SMA

| Parameter              | Value                      |
|------------------------|----------------------------|
| Reference clock inputs | 1, AC-coupled, Square Wave |

| Parameter                                                   | Value                                                     |
|-------------------------------------------------------------|-----------------------------------------------------------|
| Reference clock input voltage swing (with 50 $\Omega$ load) | $\pm 0.165$ V to $\pm 0.45$ V (0.33 V to 0.9 V peak-peak) |
| UHD driver-supported reference clock input frequencies      | 122.88 MHz, 125 MHz, or 10 MHz                            |

Table 8. PPS IN SMA

| Parameter                                                                     | Value                                                                                           |
|-------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
| PPS inputs                                                                    | 1, DC-coupled, Square Wave                                                                      |
| PPS IN I/O voltage                                                            | +3.3 V (5 V tolerant)                                                                           |
| VIL, VIH                                                                      | 0.8 V, 2.0 V                                                                                    |
| PPS IN timing versus rising edge of RefClk IN for deterministic PPS IN timing | <ul style="list-style-type: none"> <li>• &gt;3.5 ns setup</li> <li>• &gt;2.5 ns hold</li> </ul> |

## Data and System Interfaces

Table 9. Data and System Interfaces

| Parameter    | Value                                                                                                                                                                              |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CONSOLE JTAG | 2x7 2 mm shrouded header. For use with Xilinx programming cables. Provides access to FPGA JTAG. Connector is only accessible in the USRP B310 (PCIe) and USRP B310 (OEM) variants. |

## Sensors

Table 10. Sensor Names and Functions

| Sensor Name              | Description                                                                                                      | Return Value       |
|--------------------------|------------------------------------------------------------------------------------------------------------------|--------------------|
| ref_locked               | Clock reference locked. For cases using GPS to discipline the internal clock, this sensor also checks DPLL lock. | "true" or "false"  |
| temp_pcie_connector_edge | Temperature at the PCIe connector                                                                                | $^{\circ}\text{C}$ |

| Sensor Name                 | Description                                                                                                                                           | Return Value               |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|
|                             | edge. This sensor correlates closely to the shield temperature and is included in the Enclosed Thunderbolt™ variant. Not recommended to exceed 85 °C. |                            |
| temp_fpga                   | Temperature of the FPGA. Not recommended to exceed 95 °C.                                                                                             | °C                         |
| input_voltage               | Voltage at the internal Ettus USRP B310 12 V core power rail.                                                                                         | Volts                      |
| input_power                 | Power drawn from the internal Ettus USRP B310 12 V core power rail.                                                                                   | Watts                      |
| input_current               | Current drawn from the internal Ettus USRP B310 12 V core power rail.                                                                                 | Amps                       |
| lmk05318_priref_valid       | Detects if the input to the PRIREF of the LMK05318 is valid; input is connected to GPS Chip Timepulse.                                                | "valid" or "invalid"       |
| gps_pps_present             | Detects if the PPS from the LMK is toggling when there is a GPS lock.                                                                                 | "present" or "not present" |
| pcie_max_speed              | The maximum PCIe speed for the module.                                                                                                                | Speed (in GT/s)            |
| pcie_negotiated_speed       | The negotiated PCIe speed for the module.                                                                                                             | Speed (in GT/s)            |
| pcie_max_width              | The maximum PCIe link width for the module.                                                                                                           | Link Width                 |
| pcie_negotiated_width       | The negotiated PCIe link width for the module.                                                                                                        | Link Width                 |
| gps_locked                  | Whether the GPS chip is locked.                                                                                                                       | "locked" or "unlocked"     |
| gps_gpgga                   | The full NMEA GPGGA string.                                                                                                                           | NMEA string                |
| gps_time                    | Returns the GPS epoch time.                                                                                                                           | Time (in seconds)          |
| gps_gprmc                   | The full NMEA GPRMC string.                                                                                                                           | NMEA string                |
| gps_lmk04832_lock           | Returns if the LMK04832 is locked.                                                                                                                    | "locked" or "unlocked"     |
| gps_lmk05318_dpll_freq_lock | Returns if the DPLL of the LMK05318 is frequency locked.                                                                                              | "locked" or "unlocked"     |

| Sensor Name                  | Description                                           | Return Value            |
|------------------------------|-------------------------------------------------------|-------------------------|
| gps_lmk05318_dpll_phase_lock | Returns if the DPLL of the LMK05318 is phase locked.  | "locked" or "unlocked"  |
| ref_stable                   | Clock reference has remained locked since last check. | "stable" or "lost lock" |

## Programmable Logic and Baseband

Table 11. Programmable Logic

|                          |                                                                                                                                                                            |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FPGA model               | XC7K325T-1FBG676I                                                                                                                                                          |
| FPGA speed grade         | Speed Grade 1                                                                                                                                                              |
| RAM                      | 1 GB, 800 Mbps, 32 bits wide<br><br>This equates to 2.147 s of 1 channel at 125 MS/s; however, this bandwidth can be distributed across channels at supported clock rates. |
| Interfaces and protocols | PCIe Gen 2.0 x4                                                                                                                                                            |

Table 12. Baseband

|                              |                                                                                                                                                                                                                                                                                                                                         |
|------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Supported I/Q sample rates   | <p>Default I/Q Sample Rate (Master Clock Rate) applicable for RF specifications:</p> <ul style="list-style-type: none"> <li>• 122.88 MSps</li> </ul> <p>Other supported rates:</p> <ul style="list-style-type: none"> <li>• 125 MSps</li> </ul> <p>Lower rates are supported through integer resamplers in the default UHD bitfile.</p> |
| Number of available channels | 2 RX, 2 TX                                                                                                                                                                                                                                                                                                                              |

## RF Frequency

Table 13. Frequency Characteristics

|                 |                                                                                                                                                                                      |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Frequency range | <p>450 MHz to 7.125 GHz (tunable range)</p> <p>350 MHz to 7.225 GHz (tunable range with band edges by way of digital offset)</p> <p>Digital offset automatically applied by UHD.</p> |
| Frequency step  | 1 kHz                                                                                                                                                                                |

Table 14. Maximum Instantaneous Real-Time Bandwidth per Channel

|                      |         |
|----------------------|---------|
| 350 MHz to 7.225 GHz | 100 MHz |
|----------------------|---------|

## RF Transmitter



**Notice** This product is not approved or licensed for transmission over the air using a TX antenna. Operating this product with a TX antenna may violate local laws. Ensure that you comply with all local laws before operating this product with a TX antenna.

Table 15. TX Baseline Characteristics

|                                                                     |                                    |
|---------------------------------------------------------------------|------------------------------------|
| Number of channels                                                  | 2 (independent LOs shared with RX) |
| TX/RX switching time                                                | 1 $\mu$ s, nominal                 |
| Maximum reverse power when configured to TX direction, damage level | +20 dBm, nominal                   |

Table 16. TX Maximum Output Power, Typical

|                    |                 |
|--------------------|-----------------|
| 350 MHz to 700 MHz | $\geq 17.6$ dBm |
| 700 MHz to 2 GHz   | $\geq 19.2$ dBm |
| 2 GHz to 4 GHz     | $\geq 14.7$ dBm |
| 4 GHz to 6 GHz     | $\geq 10.9$ dBm |

|                   |                |
|-------------------|----------------|
| 6 GHz to 7.15 GHz | $\geq 8.6$ dBm |
|-------------------|----------------|



**Note** The values listed in [TX Maximum Output Power, Typical](#) were measured at the maximum gain setting (TX Gain = 41.5 dB) using a 0 dBFS CW signal. The output power is not leveled and can be compressed.

Table 17. TX Gain Range and Step, Nominal

|                   |         |
|-------------------|---------|
| Analog gain range | 41.5 dB |
| Analog gain step  | 0.5 dB  |

Table 18. TX Phase Noise

|                                          |               |
|------------------------------------------|---------------|
| 1 GHz center frequency, 1 kHz offset     | -106.3 dBc/Hz |
| 1 GHz center frequency, 10 kHz offset    | -118.6 dBc/Hz |
| 1 GHz center frequency, 100 kHz offset   | -121.1 dBc/Hz |
| 5.8 GHz center frequency, 1 kHz offset   | -91.2 dBc/Hz  |
| 5.8 GHz center frequency, 10 kHz offset  | -103.7 dBc/Hz |
| 5.8 GHz center frequency, 100 kHz offset | -105.4 dBc/Hz |
| 7 GHz center frequency, 1 kHz offset     | -89.7 dBc/Hz  |
| 7 GHz center frequency, 10 kHz offset    | -101.7 dBc/Hz |
| 7 GHz center frequency, 100 kHz offset   | -101.5 dBc/Hz |



**Note** The values listed in [TX Phase Noise](#) represent single-sideband phase noise, measured at TX Gain = 41.5 dB with internal reference clock.

## TX Measurements

### TX Error Vector Magnitude

Table 19. TX EVM Measurement Conditions

|                |     |
|----------------|-----|
| Link direction | UL  |
| Duplex         | FDD |

|                                                    |                                                                                              |
|----------------------------------------------------|----------------------------------------------------------------------------------------------|
| Antenna configuration                              | SISO                                                                                         |
| Bandwidth                                          | 100 MHz                                                                                      |
| Subcarrier spacing                                 | 30 kHz                                                                                       |
| Modulation                                         | 256-QAM                                                                                      |
| Frequency                                          | Tune frequency (no offset)                                                                   |
| UHD Configured Argument TxQEC Tracking Calibration | Enabled, see <i>USRP B3xx Series Hardware Driver and Device Manual</i> for more information. |

Figure 3. TX EVM Bathtub Curves, 5G NR

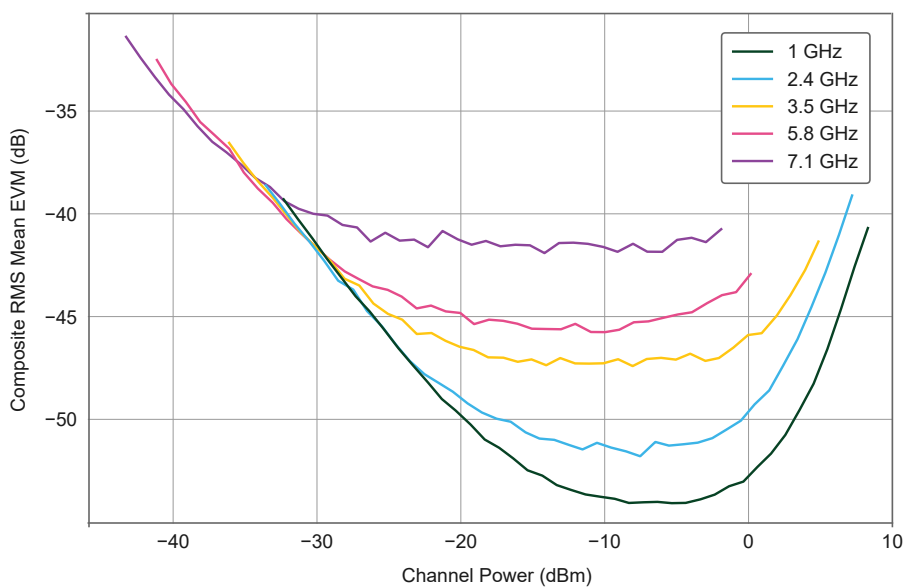
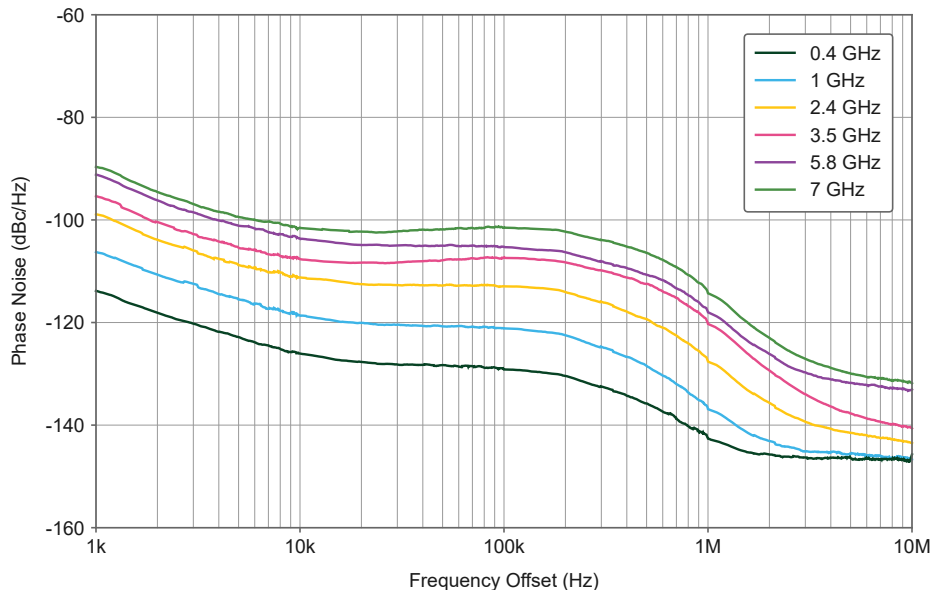


Figure 4. TX Phase Noise, Measured, MCR 122.88M



## TX Output Power



**Note** Linear output power represents output power within the linear operating region of the transmit chain. Maximum output power can be higher and can involve gain compression and increased distortion.

Table 20. TX Output Power Measurement Conditions

|                |                |
|----------------|----------------|
| Baseband level | 0 dBFS         |
| Signal type    | CW             |
| Frequency      | Tune frequency |

Figure 5. TX Maximum Output Power, Gain Setting Maximum

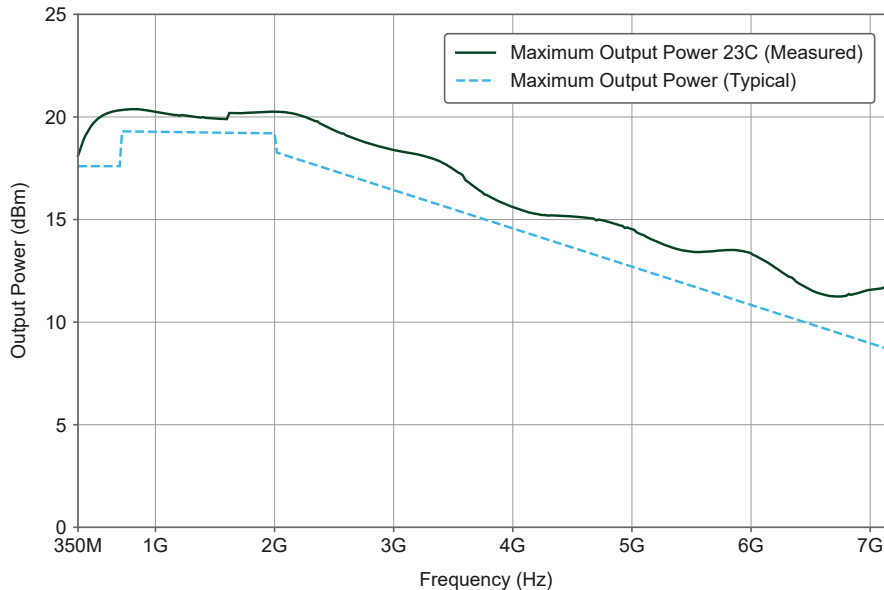
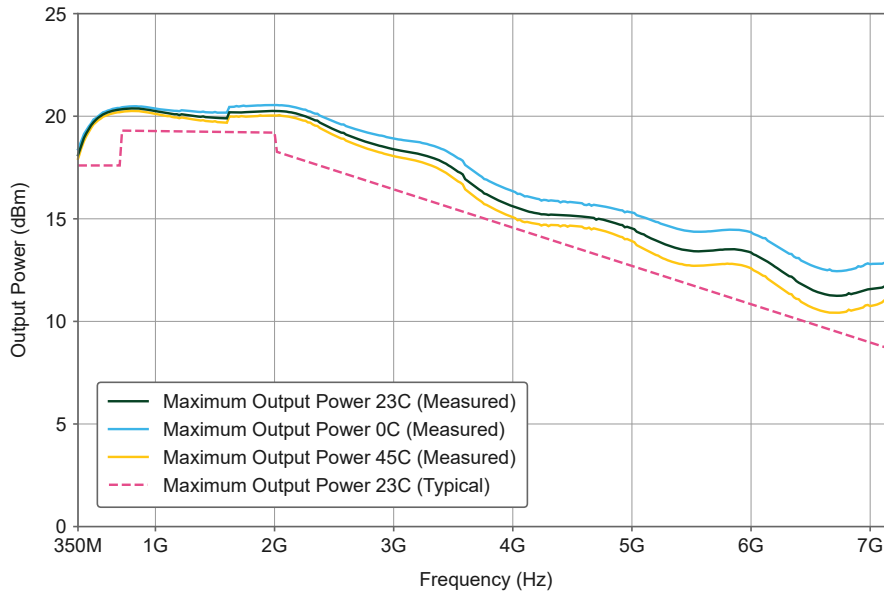


Figure 6. TX Maximum Output Power, Gain Setting Maximum, 0 °C to 50 °C



### Related information:

- [USRP B3xx Series Hardware Driver and Device Manual](#)

## RF Receiver

Table 21. RX Baseline Characteristics

|                                   |                                    |
|-----------------------------------|------------------------------------|
| Number of channels                | 2 (independent LOs shared with TX) |
| Maximum input power, damage level | +10 dBm, nominal                   |



**Notice** Supplying input power in excess of the maximum input power can result in permanent device damage.

Table 22. RX Input Power to Reach 0 dBFS, at 36 dB Gain

|                      |           |
|----------------------|-----------|
| 350 MHz to 7.125 GHz | < -16 dBm |
|----------------------|-----------|

Table 23. RX Gain Range and Step, Nominal

|            |        |
|------------|--------|
| Gain range | 36 dB  |
| Gain step  | 0.5 dB |

Table 24. RX Noise Figure

|         |         |
|---------|---------|
| 1.0 GHz | 5 dB    |
| 2.4 GHz | 5.5 dB  |
| 3.5 GHz | 6.3 dB  |
| 5.8 GHz | 8.7 dB  |
| 7.1 GHz | 10.4 dB |

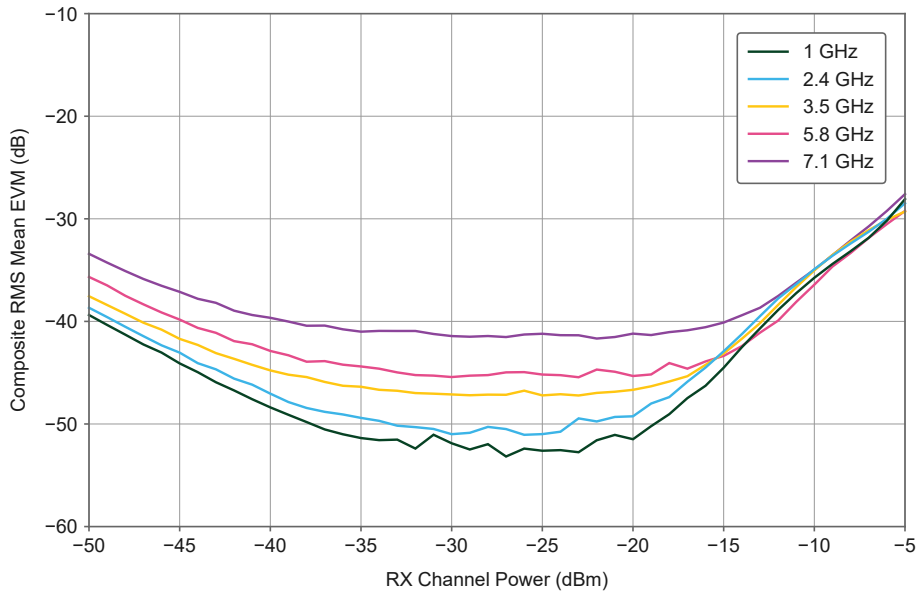
## RX Measurements

### RX Error Vector Magnitude

Table 25. RX EVM Measurement Conditions

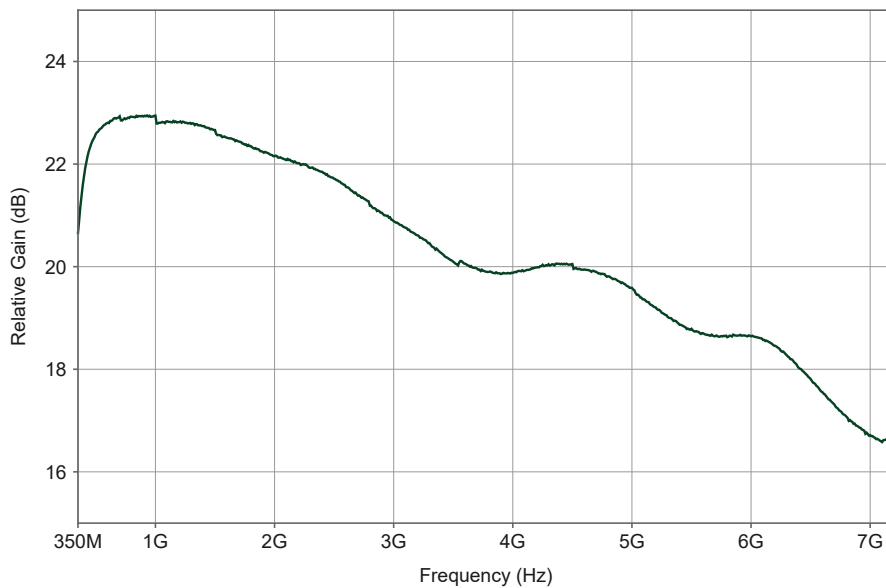
|                                                    |                                                                                              |
|----------------------------------------------------|----------------------------------------------------------------------------------------------|
| Link direction                                     | UL                                                                                           |
| Duplex                                             | FDD                                                                                          |
| Antenna configuration                              | SISO                                                                                         |
| Carrier aggregation                                | 100 MHz                                                                                      |
| MCR                                                | 125 MHz                                                                                      |
| Bandwidth                                          | 30 kHz                                                                                       |
| Subcarrier spacing                                 | 256-QAM                                                                                      |
| Modulation                                         | Tune frequency (no offset)                                                                   |
| UHD Configured Argument RxQEC Tracking Calibration | Enabled, see <i>USRP B3xx Series Hardware Driver and Device Manual</i> for more information. |

Figure 7. RX EVM Bathtub Curves, 5G NR



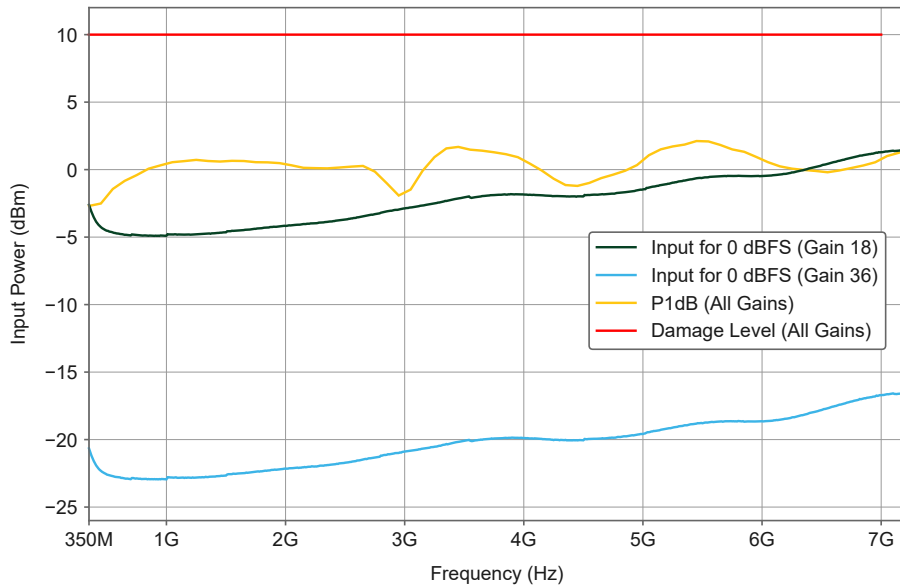
## RX Input Power

Figure 8. RX Relative Gain, at 36 dB Gain



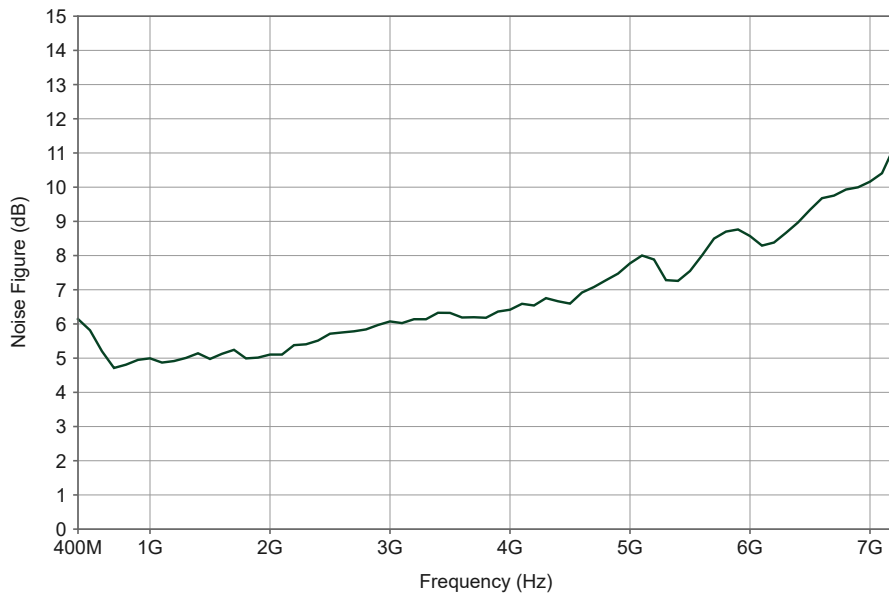
Relative gain (dB) is equal to the input power (dBm) subtracted from the measured response (dBFS).

Figure 9. RX Input Power Characterization



## RX Noise Figure

Figure 10. RX Noise Figure, at 36 dB Gain



### Related information:

- [USRP B3xx Series Hardware Driver and Device Manual](#)

## GPS Disciplined Oscillator (GPSDO)

Table 26. Frequency Accuracy

|                          |         |
|--------------------------|---------|
| TCXO (not locked to GPS) | 2.5 ppm |
| TCXO (locked to GPS)     | 5 ppb   |

Table 27. Active Antenna

|                   |                              |
|-------------------|------------------------------|
| Type              | 3.0 V active antenna         |
| Power             | 0.19 W                       |
| Frequency band(s) | L1C/A, E1-B/C, B1C 1.575 GHz |

## Power Requirements

### Power Specifications

Table 28. PCIe Gen 2.0 x4 Edge Connector

| Parameter      | Value            |
|----------------|------------------|
| Voltage rating | 12 V DC @ 2.92 A |
| Power rating   | 35 W             |

Table 29. PCIe 2x3 Power Supply Terminal (AUX Power)

| Parameter            | Value            |
|----------------------|------------------|
| Voltage rating       | 12 V DC @ 2.92 A |
| Current/power rating | 35 W             |



**Note** AUX Power is required for host devices that cannot provide at least 35 W through the PCIe Gen 2.0 x4 Edge connector.

## Phase Coherency Performance



**Note** For phase repeatability, ensure both Numerically Controlled

Oscillators (NCOs) are not in use. Additionally, you must configure the LO frequency to a multiple SYSREF:  $f_{LO} = N \cdot f_{SYSREF}$ , where  $N$  is an integer.

For example: SYSREF = 3.84 MHz for MCR = 122.88 MHz; SYSREF = 3.90625 MHz for MCR = 125 MHz.

## Definitions

- **Phase stability**—describes the short-term variation of phase and delay measured over a continuous observation window.
- **Phase repeatability**—describes the variation of phase and delay observed after configuration-changing events such as power cycles.

Table 30. Phase Coherency Performance

| Configuration                        | Measurement                       | Result     |
|--------------------------------------|-----------------------------------|------------|
| Single device (sharing internal LOs) | Phase stability                   | <0.08° RMS |
| Single device (sharing internal LOs) | Phase repeatability               | <0.3° RMS  |
| Multi-device (USRP Sync Cable)       | Phase stability                   | <1° RMS    |
| Multi-device (USRP Sync Cable)       | Phase repeatability (power cycle) | <2° RMS    |
| Multi-device (CDA-2990)              | Phase stability                   | <3° RMS    |
| Multi-device (CDA-2990)              | Phase repeatability (power cycle) | <10° RMS   |

## Environmental Guidelines



**Notice** Failure to follow the mounting instructions in the *Ettus USRP B310 User Manual* can cause temperature derating.



**Notice** Use this product indoors only.



**Notice** Apply strain relief near the input connectors of all cables. Ensure the strain relief does not cause directional bias on the cable connectors within the input connectors.



**Notice** The system integrator must provide adequate cooling for the USRP B310 (OEM). Monitor the onboard **temp\_fpga** sensor during operation and ensure the FPGA temperature remains below 95 °C. Additional airflow, heatsinking, or enclosure ventilation might be required depending on the application and ambient operating conditions.

## Environmental Characteristics



**Note** In order to ensure safe operation of the USRP B310 (OEM) in end-use equipment, you must not exceed the temperature for the components in the following table. Monitor the temperature using the built-in Ettus USRP B310 FPGA temperature sensor. Do not let the temperature sensor exceed 95 °C. Refer to the *USRP Hardware Driver and Device Manual* for additional information on reading this sensor.



**Notice** Several factors greatly influence the USRP B310 (OEM) thermal performance. These factors include resource utilization, mounting, and adjacent power dissipation. These factors can substantially affect the achievable external ambient temperature at which the maximum local and reported temperatures are reached. NI recommends you validate your system to ensure local and reported temperatures remain within maximum allowed temperature ranges. In some applications, additional thermal design might be necessary.

Table 31. Temperature

| Parameter                          | Value           |
|------------------------------------|-----------------|
| Operating temperature <sup>2</sup> | -20 °C to 45 °C |

2. The operating temperature is the recommended ambient temperature around the product with the PCIe variant integration (NI Part Number: 790817-01—PCIe). Higher operating temperatures might be achieved with active cooling such as fans or liquid cooling.

| Parameter                       | Value                                                                                                                                            |
|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Storage temperature             | -40 °C to 85 °C                                                                                                                                  |
| PCIe connector edge temperature | <ul style="list-style-type: none"> <li>85 °C maximum</li> <li>PCIe connector edge temperature sensor name: "temp_pcie_connector_edge"</li> </ul> |
| FPGA temperature                | <ul style="list-style-type: none"> <li>95 °C maximum</li> <li>FPGA temperature sensor name: "temp_fpga"</li> </ul>                               |

Table 32. Humidity

| Parameter          | Value                               |
|--------------------|-------------------------------------|
| Operating humidity | 10% to 90% relative, non-condensing |
| Storage humidity   | 5% to 95% relative, non-condensing  |

Table 33. Pollution Degree

| Parameter        | Value |
|------------------|-------|
| Pollution Degree | 2     |

Table 34. Maximum Altitude

| Parameter        | Value   |
|------------------|---------|
| Maximum altitude | 2,000 m |